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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/573,458	03/24/2006	Koji Otsuka	SHG-046P2-319/OSP-19842	2611
26875 7590 11/26/2008 WOOD, HERRON & EVANS, LLP 2700 CAREW TOWER 441 VINE STREET CINCINNATI, OH 45202				
EXAMINER				
ROLAND, CHRISTOPHER M				
ART UNIT		PAPER NUMBER		
2893				
MAIL DATE		DELIVERY MODE		
11/26/2008		PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/573,458

**Applicant(s)**

OTSUKA ET AL.

**Examiner**

Christopher M. Roland

**Art Unit**

2893

**Period for Reply** -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 August 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-4, 6 and 8-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6 and 8-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 August 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB-08)
- Paper No(s)/Mail Date \_\_\_\_\_

- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Status of the Claims***

1. Amendment filed 14 August 2008 is acknowledged. **Claims 5 and 7** have been cancelled. **Claims 1-4, 6, and 8** have been amended. **Claim 11** has been added. **Claims 1-4, 6, and 8-11** are pending.

### ***Drawings***

2. Amendments to the drawings filed 14 August 2008 are acknowledged.

### ***Specification***

3. Amendments to the specification filed 14 August 2008 are acknowledged.

### ***Claim Objections***

4. **Claim 3** is objected to because of the following informalities: there is insufficient antecedent basis for the limitation, "the interface," in the claim. Appropriate correction is required.
5. **Claims 4 and 11** are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim should refer to other claims in the alternative only. See MPEP § 608.01(n).

6. **Claim 11** is objected to because of the following informalities: there is insufficient antecedent basis for the limitation, "the forward current," in the claim. Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. **Claims 1-4, 6, and 8-11** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-3 recite the limitation, "a first concave portion...that faces the interface between the first semiconductor layer and the second semiconductor layer." It is unclear from the disclosure how the concave portion faces the interface, what surface faces the interface, or how the concave portion may face the interface even as it extends deeper than said interface.

Claim 11 recites the limitation, "wherein the forward current can be restricted when voltage is applied from the first electrode to the second electrode, and desirable voltage resistance characteristics occur when voltage is applied in the reverse direction." This is in marked contrast to Applicant's specification, which discloses, "When voltage is applied in the forward direction (for example, when a positive charge is applied to the electrode 15 and a negative charge is applied to the electrode 16), then current flows from the electrode 15 to the two-dimensional carder 102 to the electrode

16, as is shown by the arrow in FIG. 1," and, "When voltage is applied in the reverse direction, the electrical contact between the two-dimensional carder 102 and the electrode 15 is broken, and it becomes difficult for current to flow between the two-dimensional carder 102 and the electrode 15," (p. 10, ln. 16 - p. 11, ln. 17). The claim, as presently recited, makes no distinction between a positive voltage and a negative voltage, or alternatively a voltage applied in a forward direction and a voltage applied in a reverse direction, between the two electrodes. This distinction must be made in order to make clear the device operation as described in the specification. Further, the limitation, "desirable voltage resistance characteristics," is vague and indefinite because desirable characteristics are application-specific.

Claims 4, 6, and 8-10 are rejected for merely containing the flaw(s) of the parent claim.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. **Claims 3 and 11** are rejected under 35 U.S.C. 102(b) as being anticipated by Peatman et al. ("A Novel Schottky/2-DEG Diode for Millimeter- and Submillimeter-Wave Multiplier Applications," hereinafter Peatman).

With respect to claim 3, as best understood by Examiner, Peatman teaches (FIG. 1) a semiconductor device as claimed, comprising:

a first semiconductor layer (GaAs layer) that is formed from a first semiconductor material (p. 12, col. 1, ln. 32-48);

a second semiconductor layer (AlGaAs layer) that is formed from a second semiconductor material above the first semiconductor layer (p. 12, col. 1, ln. 32-48);

a third semiconductor layer (InGaAs layer) that is sandwiched between the first semiconductor layer and the second semiconductor layer and that is formed having a thickness that allows a quantum mechanical tunnel effect to be obtained (p. 12, col. 1, ln. 32-48);

a two-dimensional carrier (2-DEG) that is formed within the first semiconductor layer and on the third semiconductor layer side of the first semiconductor layer (p. 12, col. 1, ln. 32-48);

a first concave portion (trench) that is formed penetrating at least the second semiconductor layer from a primary surface of the second semiconductor layer that faces the interface between the third semiconductor layer and the second semiconductor layer, and is formed from the interface to a predetermined depth in the first semiconductor layer (p. 12, col. 1, ln. 32-48);

a first electrode (Schottky contact) that is formed on a bottom surface and side surface of the first concave portion and that forms a Schottky junction with the semiconductor layers which contact the bottom surface and the side surface of the first concave portion (p. 12, col. 1, ln. 32-48); and

a second electrode (ohmic contact) that is formed in an area of the second semiconductor layer that is located away from the first electrode and that forms a low resistance contact with the second semiconductor layer (p. 12, col. 1, ln. 32-48).

With respect to claim 11, as best understood by Examiner, Peatman teaches wherein the forward current can be restricted when voltage is applied from the first electrode to the second electrode, and desirable voltage resistance characteristics occur when voltage is applied in the reverse direction (p. 12, col. 1, ln. 32-48).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. **Claims 1, 2, and 8-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Peatman in view of Kanazawa (Japanese Patent Application Publication 03-016179, hereinafter Kanazawa '179) of record.

With respect to claim 1, as best understood by Examiner, Peatman teaches (FIG. 1) a semiconductor device substantially as claimed, comprising:

a first semiconductor layer (GaAs layer) that is formed from a first semiconductor material (p. 12, col. 1, ln. 32-48);

a second semiconductor layer (AlGaAs layer) that is formed from a second semiconductor material on the first semiconductor layer (p. 12, col. 1, ln. 32-48);

a two-dimensional carrier (2-DEG) that is formed within the first semiconductor layer and in the vicinity of an interface (p. 12, col. 1, ln. 32-48);

a first concave portion (trench) that is formed penetrating at least the second semiconductor layer from a primary surface of the second semiconductor layer that faces the interface, and is formed from the interface to a predetermined depth in the first semiconductor layer (p. 12, col. 1, ln. 32-48);

a first electrode (Schottky contact) that is formed on a bottom surface and side surface of the first concave portion and that forms a Schottky junction to the semiconductor layers which contact the bottom surface and the side surface of the first concave portion (p. 12, col. 1, ln. 32-48); and

a second electrode (ohmic contact) that is formed in an area of the second semiconductor layer that is located away from the first electrode and that forms a low resistance contact with the second semiconductor layer (p. 12, col. 1, ln. 32-48).

Thus, Peatman is shown to teach all the features of the claim with the exception of an interface between the first semiconductor layer and the second semiconductor layer.

However, Kanazawa '179 teaches (FIG. 1) an AlGaAs layer (11) directly above a GaAs layer (10) to generate a two-dimensional electron gas in a device whose conversion loss and noise factor are small (abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the interface of the device of Peatman without an InGaAs layer as taught by Kanazawa '179 such that the AlGaAs layer forms an interface with the GaAs layer to generate a two-dimensional electron gas in a device whose conversion loss and noise factor are small.

With respect to claim 2, as best understood by Examiner, Peatman teaches a semiconductor device substantially as claimed, comprising:

- a first semiconductor layer (GaAs layer) that is formed from a first semiconductor material (p. 12, col. 1, ln. 32-48);

- a second semiconductor layer (AlGaAs layer) that is formed from a second semiconductor material on the first semiconductor layer (p. 12, col. 1, ln. 32-48);

- a two-dimensional carrier (2-DEG) that is formed within the first semiconductor layer and in the vicinity of an interface (p. 12, col. 1, ln. 32-48);

- a first concave portion (trench) that is formed from a primary surface of the second semiconductor layer that faces the interface reaching at least the interface, and is formed to a distance that allows a quantum mechanical tunnel effect with the two dimensional carrier to be obtained (p. 12, col. 1, ln. 32-48);

- a first electrode (Schottky contact) that is formed on a bottom surface and a side surface of the first concave portion and that forms a Schottky junction to the semiconductor layers which contact the bottom surface and side surface of the first concave portion (p. 12, col. 1, ln. 32-48); and

a second electrode (ohmic contact) that is formed in an area of the second semiconductor layer that is located away from the first electrode and that forms a low resistance contact with the second semiconductor layer (p. 12, col. 1, ln. 32-48).

Thus, Peatman is shown to teach all the features of the claim with the exception of an interface between the first semiconductor layer and the second semiconductor layer.

However, Kanazawa '179 teaches (FIG. 1) an AlGaAs layer (11) directly above a GaAs layer (10) to generate a two-dimensional electron gas in a device whose conversion loss and noise factor are small (abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the interface of the device of Peatman without an InGaAs layer as taught by Kanazawa '179 such that the AlGaAs layer forms an interface with the GaAs layer to generate a two-dimensional electron gas in a device whose conversion loss and noise factor are small.

With respect to claims 8-10, Peatman teaches the device as described in claim 1 above with the exception of the additional limitations:

wherein, when viewed from a perpendicular direction relative to the primary surface, the second electrode surrounds the first electrode, and the inner surface of the second electrode is formed so as to face the outer surface of the first electrode;

wherein, when viewed from a perpendicular direction relative to the primary surface, the second electrode is formed so as to surround the first electrode; and

wherein the first electrode is also formed on the primary surface of the second semiconductor layer that surrounds the first concave portion.

However, Kanazawa '179 teaches (FIG. 1) ohmic second electrodes (13) surrounding a Schottky first electrode (12) wherein the first electrode is formed on the primary surface of the second semiconductor layer in a device whose conversion loss and noise factor are small (abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the second electrodes of Peatman to surround the first electrode on the primary surface of the second semiconductor layer as taught by Kanazawa '179 in a device whose conversion loss and noise factor are small.

With respect to claim 11, as best understood by Examiner, Peatman teaches wherein the forward current can be restricted when voltage is applied from the first electrode to the second electrode, and desirable voltage resistance characteristics occur when voltage is applied in the reverse direction (p. 12, col. 1, ln. 32-48).

10. **Claims 4 and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Peatman and Kanazawa '179 as applied to claims 1 and 2 above, and further in view of Patel et al. (UK Patent Application Publication 2 279 806, hereinafter Patel '806) of record.

With respect to claims 4 and 6, Peatman and Kanazawa '179 teach the device as described in claims 1 and 2 above with the exception of the additional limitations:

wherein there is further provided a second concave portion that is formed from the primary surface of the second semiconductor layer penetrating at least the second semiconductor layer and is formed from the interface to a predetermined depth in the first semiconductor layer, and wherein

the second electrode is formed on a bottom surface and side surface of the second concave portion, and forms a low resistance contact with the semiconductor layers which contact the bottom surface and side surface of the second concave portion; and

wherein the second electrode is formed from the primary surface of the second semiconductor layer to the two-dimensional carrier.

However, Patel '806 teaches forming ohmic contact layers (33) in concave portions extending beyond the interface of two semiconductor layers to the 2-DEG (15) (p. 7, ln. 21—p. 8, ln. 24) in a method to form shallow ohmic contacts extending directly to the active layer of interest in a heterojunction semiconductor device (p. 5, ln. 12-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the second electrode of Peatman and Kanazawa '179 in a concave portion to the two-dimensional carrier as taught by Patel '806 to form shallow ohmic contacts extending directly to the active layer of interest in a heterojunction semiconductor device.

11. **Claims 4 and 6** rejected under 35 U.S.C. 103(a) as being unpatentable over Peatman as applied to claim 3 above, and further in view of Patel '806.

With respect to claims 4 and 6, Peatman teaches the device as described in claim 3 above with the exception of the additional limitations:

wherein there is further provided a second concave portion that is formed from the primary surface of the second semiconductor layer penetrating at least the second semiconductor layer and is formed from the interface to a predetermined depth in the first semiconductor layer, and wherein

the second electrode is formed on a bottom surface and side surface of the second concave portion, and forms a low resistance contact with the semiconductor layers which contact the bottom surface and side surface of the second concave portion; and

wherein the second electrode is formed from the primary surface of the second semiconductor layer to the two-dimensional carrier.

However, Patel '806 teaches forming ohmic contact layers (33) in concave portions extending beyond the interface of two semiconductor layers to the 2-DEG (15) (p. 7, ln. 21—p. 8, ln. 24) in a method to form shallow ohmic contacts extending directly to the active layer of interest in a heterojunction semiconductor device (p. 5, ln. 12-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the second electrode of Peatman in a concave portion to the two-dimensional carrier as taught by Patel '806 to form shallow ohmic contacts extending directly to the active layer of interest in a heterojunction semiconductor device.

12. **Claims 8-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Peatman as applied to claim 3 above, and further in view of Kanazawa '179.

With respect to claims 8-10, Peatman teaches the device as described in claim 3 above with the exception of the additional limitations wherein, when viewed from a perpendicular direction relative to the primary surface, the second electrode surrounds the first electrode, and the inner surface of the second electrode is formed so as to face the outer surface of the first electrode; wherein, when viewed from a perpendicular direction relative to the primary surface, the second electrode is formed so as to surround the first electrode; and wherein the first electrode is also formed on the primary surface of the second semiconductor layer that surrounds the first concave portion.

However, Kanazawa '179 teaches ohmic electrodes (13) surrounding a Schottky electrode (12), wherein the Schottky electrode is formed on the primary surface of the second semiconductor layer (11) in a device whose conversion loss and noise factor are small (abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the second electrode of Peatman to surround the first electrode as taught by Kanazawa '179; and to have formed the first electrode in the concave portion of Peatman on the primary surface of the second semiconductor as taught by Kanazawa '179 in a device whose conversion loss and noise factor are small.

***Response to Arguments***

13. Applicant's amendments to the drawings and the specification are sufficient to overcome the objections made in the non-final rejection filed 14 May 2008. The objections to the drawings and the specification have been withdrawn.

14. Applicant's amendments to claims 1-4, 6, and 8 are sufficient to overcome some of the 35 USC § 112 2<sup>nd</sup> paragraph rejections made in the non-final rejection filed 14 May 2008. Some of the 35 USC § 112 2<sup>nd</sup> paragraph rejections of claims 1-10 have been withdrawn.

15. Applicant's arguments filed 14 August 2008 with respect to the remaining 35 USC § 112 2<sup>nd</sup> paragraph rejection of claims 1-10 have been fully considered but they are not persuasive.

Applicant argues (remarks, pp. 10-12) that the newly presented limitations of claims 1-3 are sufficient to overcome the 35 USC § 112 2<sup>nd</sup> paragraph rejections of claims 1 and 3 as set forth in the non-final rejection filed 14 May 2008. Examiner respectfully disagrees.

Examiner maintains that it is unclear how a concave portion may face an interface. A concave portion usually has a plurality of surfaces, many of said surfaces capable of facing a different direction. It is unclear how a concave portion, when taken as a whole, faces an interface.

16. Applicant's arguments with respect to the Margalit '823 and Fukuzawa '925 references as cited in the rejections of claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

17. Applicant's arguments filed 14 August 2008 with respect to the Patel '806 reference cited in the rejections of claims 6 and 7 have been fully considered but they are not persuasive.

Applicant argues (remarks, p. 16) that an Ohmic electrode is formed in a concave portion in Patel, but it fails to form a Schottky electrode in a concave portion.

Patel '806 teaches the claimed ohmic contact layers (33) extending beyond the interface of two semiconductor layers to the 2-DEG (15) (p. 7, ln. 21—p. 8, ln. 24). Peatman is cited to teach the claimed Schottky electrode.

### ***Conclusion***

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Beach (US Patent Application Publication 2006/0006413);

Yanagihara et al. (US Patent Application Publication 2006/0108659);

Koh et al. ("Millimeter Wave Tripler Evaluation of a Metal/2-DEG Schottky Diode Varactor");

Castro et al. ("Schottky Contact between Metal and Two-Dimensional Electron Gas: Device Applications to Low-Noise Optical Detectors"); and

Anwar et al. ("Barrier Enhancement Mechanisms in Heterodimensional Contacts and their Effect on Current Transport") teach devices having Schottky and ohmic contacts.

Ogawa (US Patent 5,099,295); and

Daniels et al. ("Quantum-Well p-Channel AlGaAs/InGaAs/GaAs Heterostructure Insulated-Gate Field-Effect Transistors with Very High Transconductance") teach AlGaAs/InGaAs/GaAs devices.

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher M. Roland whose telephone number is 571-270-1271. The examiner can normally be reached on Monday-Friday, 8:00AM-5:00PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. M. R./  
Examiner, Art Unit 2893

/Davienne Monbleau/  
Supervisory Patent Examiner, Art Unit 2893